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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,741	08/18/2003	Steven L. Scott	1376.733US1	4093

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/643,741	SCOTT ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply.

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/14/04, 2/21/06, 6/12/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/643,741 has a total of 23 claims pending in the application, there are 3 independent claims and 20 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings submitted August 18, 2003 are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3. Applicant is reminded that an applicant's duty of disclosure of material and information is not satisfied by presenting a patent examiner with *"a mountain of largely irrelevant (material) from which he is presumed to have been able, with his expertise and with adequate time, to have found the critical (material). It ignores the real world conditions under which examiners work." See Rohm & Haas Co. v. Crystal Chemical Co.*, 722 F.2d 1556, 1573 (220 USPQ 289) (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) (Emphasis in original).

Patent applicant has a duty not just to disclose pertinent prior art references but to make a disclosure in such way as not to "bury" it within other disclosures of less relevant prior art; *See Golden Valley Microwave Foods Inc. v. Gealer Popcorn Co. Inc.*, 24 USPQZd 1801 (N.D. Ind. 1992)., *Molins PLC v. Textron Inc.* 26 USPQZd 1889, at 1899 (D.Del. 1992)., *Penn Yan Boats, Inc. v. Sea Lark Boats, Inc. et al.*, 175 USPQ 260, at 272 (S.D. Fl. 1972).

Eliminate clearly irrelevant and marginally pertinent cumulative information. If a long list is submitted, highlight those documents which have been specifically brought to applicant's attention and/or are known to be of most significance. *See Penn Yan Boats, Inc. v. Sea Lark Boats, Inc.*, 359 F. Supp. 948, 175 USPQ 260 (S.D. Fla. 1972), aff 'd, 479 F.2d 1338, 178 USPQ 577 (5th Cir. 1973), cert. denied, 414 U.S. 874 (1974). But cf. *Molins PLC v. Textron Inc.*, 48 F.3d 1172, 33 USPQZd 1823 (Fed. Cir. 1995).

Please note that it is Applicant's duty to particularly point out any highly relevance material amongst the references cited in the IDS. A cursory review of the submitted references was performed by the Examiner under the condition noted above.

OBJECTIONS

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which Applicant may become aware in the specification.

Claims

5. **Claims 19 and 22** objected to because of the following informalities:

6. **As per claim 19**, the limitation "queueing" in line 2 should instead read "queuing."

7. **As per claim 22**, the limitation "inserting to first" in line 2 should instead read "inserting to the first."

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. **As per claims 1, 11, and 21**, the limitation "one or memory requests" is vague and indefinite. For the purposes of examining the instant application the Examiner will interpret the limitation to instead read "one or more memory requests."

11. **Also per claims 3, 4, 13, 14, and 23**, the claims recite the limitation "the first synchronization instruction." There is insufficient antecedent basis for this limitation in the claims. For the purposes of examining the instant application the Examiner will interpret the limitation to refer to "a second instruction that specifies a synchronization operation" as recited in claims 1, 11, 21.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. **Claims 1, 11, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al. (U.S. Patent Application Publication 2002/0116600).**

14. **As per claim 1**, Smith discloses an apparatus comprising:

a first plurality of queues, including a first queue and a second queue, each of the first plurality of queues for holding a plurality of pending memory requests (paragraph 0077; Fig. 6A); *It should be noted that thread 0 within the reorder buffer is analogous to the "first queue" and thread 1 within the reorder buffer is analogous to the "second queue." It should also be noted that the "microinstructions" are analogous to "memory requests."*

one or more instruction-processing circuits, operatively coupled to the plurality of queues, that inserts one or memory requests into at least one of the queues based on a first instruction that specifies a memory operation, and that inserts a first synchronization marker into the first queue and inserts a second synchronization marker into the second queue based on a second instruction that specifies a synchronization operation, and that inserts one or memory requests into at least one of the queues based on a third instruction that specifies a memory operation (paragraph 0039; paragraph 0100; Fig. 2, element 66); *It should be noted that the "microcode sequencer" is analogous to the "instruction-processing circuits" and the "macroinstructions" are analogous to the "first, second, and third instructions."*

and a first synchronization circuit, operatively coupled to the first plurality of queues, that selectively halts processing of further memory requests from the first queue based on the first synchronization marker reaching a predetermined point in the first queue until the corresponding second synchronization marker reaches a predetermined point in the second queue (paragraph 0100; paragraph 0103; paragraph

0109; Fig. 6A, element 188; Fig. 7A, elements 222, 270, and 288). *It should be noted that the "event handler" is analogous to the "synchronization circuit."*

15. **As per claim 11**, Smith discloses a method comprising:

providing a first plurality of queues, including a first queue and a second queue, each of the first plurality of queues for holding a plurality of pending memory requests (paragraph 0077; Fig. 6A);

inserting one or memory requests into at least one of the queues based on a first instruction that specifies a memory operation (paragraph 0039; paragraph 0100; Fig. 2, element 66);

based on a second instruction that specifies a synchronization operation inserting a first synchronization marker into the first queue and inserting a second synchronization marker into the second queue (paragraph 0039; paragraph 0100; Fig. 2, element 66);

inserting one or memory requests into at least one of the queues based on a third instruction that specifies a memory operation (paragraph 0039; paragraph 0100; Fig. 2, element 66);

processing memory requests from the first queue (paragraph 0079; Fig. 2, element 70);

and selectively halting further processing of memory requests from the first queue based on the first synchronization marker reaching a predetermined point in the first queue until the corresponding second synchronization marker reaches a

predetermined point in the second queue (paragraph 0100; paragraph 0103; paragraph 0109; Fig. 6A, element 188; Fig. 7A, elements 222, 270, and 288).

16. **As per claim 21**, Smith discloses an apparatus comprising:

a first plurality of queues, including a first queue and a second queue, each of the first plurality of queues for holding a plurality of pending memory requests (paragraph 0077; Fig. 6A);

means for inserting one or memory requests into at least one of the queues based on a first instruction that specifies a memory operation (paragraph 0039; paragraph 0100; Fig. 2, element 66);

means for, based on a second instruction that specifies a synchronization operation inserting a first synchronization marker into the first queue and inserting a second synchronization marker into the second queue (paragraph 0039; paragraph 0100; Fig. 2, element 66);

means for inserting one or memory requests into at least one of the queues based on a third instruction that specifies a memory operation (paragraph 0039; paragraph 0100; Fig. 2, element 66);

means for processing memory requests from the first queue (paragraph 0079; Fig. 2, element 70);

and means for selectively halting further processing of memory requests from the first queue based on the first synchronization marker reaching a predetermined point in the first queue until the corresponding second synchronization marker reaches a

predetermined point in the second queue (paragraph 0100; paragraph 0103; paragraph 0109; Fig. 6A, element 188; Fig. 7A, elements 222, 270, and 288).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 2-6, 9-10, 12-16, 19-20, and 22-23 are rejected under 35 U.S.C. 103(a) as being obvious over Smith in view of Chen et al. (U.S. Patent 5,197,130).

19. **As per claim 2**, Smith discloses the plurality of queues is within a processor (paragraph 0038; Fig. 2).

the first queue is used for synchronizations, and the second queue is used for synchronizations (paragraph 0077; Fig. 6A, elements 180 and 186).

Smith does not expressly disclose the first queue is used only for vector memory requests and the second queue is used only for scalar memory requests.

Chen discloses the first queue is used only for vector memory requests and the second queue is used only for scalar memory requests (col. 10, line 65 – col. 11, line 17; Fig. 4).

Smith and Chen are analogous art because they are from the same field of endeavor, that being processor systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Chen's vector and scalar processing means with Smith's multithreaded processor to create a multiprocessor cluster.

The motivation for doing so would have been to increase system performance by providing a multiprocessor cluster of tightly-coupled, high-speed processors capable of both vector and scaler parallel processing that can symmetrically access shared resources (Chen, col. 6, line 65 – col. 7, line 1).

Therefore, it would have been obvious to combine Smith and Chen for the benefit of obtaining the invention as specified in claim 2.

20. **As per claim 3**, the combination of Smith/Chen discloses the first synchronization instruction is an Lsync-type instruction (Smith, paragraph 0039; paragraph 0100). *It should be noted that the synchronization takes place with the local memory.*

21. **As per claim 4**, the combination of Smith/Chen discloses the first synchronization instruction is an Lsync V,S-type instruction (Chen, col. 23, lines 17-46).

22. **As per claim 5**, the combination of Smith/Chen discloses for a second synchronization instruction, a corresponding synchronization marker is inserted to only the first queue (Smith, paragraph 0100; paragraph 0104; Fig. 7A, element 272).

23. **As per claim 6**, the combination of Smith/Chen discloses the first synchronization instruction is an Lsync-type instruction (Smith, paragraph 0039; paragraph 0100).

24. **As per claim 9**, the combination of Smith/Chen discloses a fifth queue for holding a plurality of write data elements, wherein each write data element corresponds to a memory request in the first queue, and wherein the write data elements are loaded into the fifth queue decoupled from the loading of memory requests into the first queue (Chen, col. 17, lines 55-58; col. 18, lines 13-30; Fig. 14, element 326). *It should be noted that the "data queue" is analogous to the "fifth queue."*

25. **As per claim 10**, the combination of Smith/Chen discloses a data cache (Smith, paragraph 0054; Fig. 3, element 88);

an external cache, wherein first synchronization instruction is an Lsync V,S type instruction, preventing subsequent scalar references from accessing the data cache until all vector references have been sent to the external cache and all vector writes have caused any necessary invalidations of the data cache (Chen, col. 12, lines 14-28; Fig. 5, element 110).

26. **As per claim 12**, Smith discloses the plurality of queues is within a first processor (paragraph 0038; Fig. 2).

and the inserting to the first queue is for synchronizations, and the inserting to the second queue is for synchronizations (paragraph 0077; Fig. 6A, elements 180 and 186).

Smith does not expressly disclose the inserting to the first queue is for only vector memory requests and the inserting to the second queue is for only scalar memory requests.

Chen discloses the inserting to the first queue is for only vector memory requests and the inserting to the second queue is for only scalar memory requests (col. 10, line 65 – col. 11, line 17; Fig. 4).

Please see the 103 rejection of claim 2 above (Smith in view of Chen) for the reasons to combine Smith and Chen.

27. **As per claim 13**, the combination of Smith/Chen discloses the first synchronization instruction is an Lsync-type instruction (Smith, paragraph 0039; paragraph 0100).

28. **As per claim 14**, the combination of Smith/Chen discloses the first synchronization instruction is an Lsync V,S-type instruction (Chen, col. 23, lines 17-46).

29. **As per claim 15**, the combination of Smith/Chen based on a second synchronization instruction that specifies a synchronization operation, inserting a corresponding synchronization to only the first queue (Smith, paragraph 0100; paragraph 0104; Fig. 7A, element 272).

30. **As per claim 16**, the combination of Smith/Chen discloses the first synchronization instruction is an Lsync-type instruction (Smith, paragraph 0039; paragraph 0100).

31. **As per claim 19**, the combination of Smith/Chen discloses queueing a plurality of write data elements to a fifth queue, wherein each write data element corresponds to a memory request in the first queue, and wherein the write data elements are inserted into the fifth queue decoupled from the inserting of memory requests into the first queue (Chen, col. 17, lines 55-58; col. 18, lines 13-30; Fig. 14, element 326).

32. **As per claim 20**, the combination of Smith/Chen discloses providing a data cache and an external cache, wherein first synchronization instruction is an Lsync V,S type instruction (Smith, paragraph 0054; Fig. 3, element 88; Chen, col. 12, lines 14-28; Fig. 5, element 110).

and preventing subsequent scalar references from accessing the data cache until all vector references have been sent to the external cache and all vector writes have caused any necessary invalidations of the data cache based on the first synchronization instruction (Chen, col. 12, lines 14-28).

33. **As per claim 22**, Smith discloses the plurality of queues is within a first processor (paragraph 0038; Fig. 2).

and the means for inserting to the first queue is for synchronizations, and the means for inserting to the second queue is for synchronizations (paragraph 0077; Fig. 6A, elements 180 and 186).

Smith does not expressly disclose the means for inserting to the first queue is for only vector memory requests and the means for inserting to the second queue is for only scalar memory requests.

Chen discloses the means for inserting to the first queue is for only vector memory requests and the means for inserting to the second queue is for only scalar memory requests (col. 10, line 65 – col. 11, line 17; Fig. 4).

Please see the 103 rejection of claim 2 above (Smith in view of Chen) for the reasons to combine Smith and Chen.

34. **As per claim 23**, the combination of Smith/Chen discloses the first synchronization instruction is an Lsync-type instruction (Smith, paragraph 0039; paragraph 0100).

35. Claims 7-8 and 17-18 are rejected under 35 U.S.C. 103(a) as being obvious over Smith in view of Barnes et al. (U.S. Patent 4,412,303).

36. **As per claim 7**, Smith discloses all the limitations of claim 7 except a second plurality of queues, including a third queue and a fourth queue, each of the second plurality of queues for holding a plurality of pending memory requests; wherein the plurality of queues is in a circuit coupled to each of a plurality of processors including a first processor and a second processor, and wherein the third queue is used for only memory requests and synchronizations from the first processor, and the second queue is used for only memory requests and synchronizations from the second processor.

Barnes discloses a second plurality of queues, including a third queue and a fourth queue, each of the second plurality of queues for holding a plurality of pending memory requests; wherein the plurality of queues is in a circuit coupled to each of a plurality of processors including a first processor and a second processor, and wherein the third queue is used for only memory requests and synchronizations from the first processor, and the second queue is used for only memory requests and synchronizations from the second processor (col. 5, lines 50-55; col. 6, lines 4-31 and 39-55; Fig. 1, elements 23 and 29). *It should be noted that the "proc. 0" analogous to the "first processor", "proc. 1" is analogous to the "second processor", the "connection*

network buffer" within proc. 0 is analogous to the "third queue", and the "connection network buffer" within proc. 1 is analogous to the "fourth queue."

Smith and Barnes are analogous art because they are from the same field of endeavor, that being processor systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Barnes' array processor architecture with Smith's multithreaded processor to create a parallel processing array.

The motivation for doing so would have been to efficiently process vector and other data elements in a parallel but not a locked-step fashion (Barnes, col. 2, lines 48-50).

Therefore, it would have been obvious to combine Smith and Barnes for the benefit of obtaining the invention as specified in claim 7.

37. **As per claim 8**, the combination of Smith/Barnes discloses a second synchronization circuit, operatively coupled to the second plurality of queues, that selectively halts further processing of memory requests from the third queue based on the first synchronization marker reaching a predetermined point in the third queue until a corresponding synchronization marker from the second processor reaches a predetermined point in the fourth queue (Barnes, col. 7, lines 28-47; Fig. 3, element 21). *It should be noted that the "coordinator" is analogous to the "second synchronization circuit."*

38. **As per claim 17**, the combination of Smith/Barnes discloses providing a plurality of processors including a first processor and a second processor (Barnes, col. 5, lines 50-55; Fig. 1, elements 29);

providing a second plurality of queues, including a third queue and a fourth queue, each of the second plurality of queues for holding a plurality of pending memory requests (Barnes, col. 6, lines 39-55; Fig. 1, elements 23);

inserting to the third queue only memory requests and synchronizations from the first processor (Barnes, col. 6, lines 4-31 and 39-55);

and inserting to the second queue only memory requests and synchronizations from the second processor (Barnes, col. 6, lines 4-31 and 39-55).

39. **As per claim 18**, the combination of Smith/Barnes discloses selectively halting further processing of memory requests from the third queue based on the first synchronization marker reaching a predetermined point in the third queue until a corresponding synchronization marker from the second processor reaches a predetermined point in the fourth queue (Barnes, col. 7, lines 28-47; Fig. 3, element 21).

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-23** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 4,989,131 (Stone) discloses a parallel synchronization technique utilizing a combining network in which two processors synchronize by having one processor suspend operation while the other processor becomes the agent for the one processor, while continuing to operate on its own behalf.

2. U.S. Patent 6,496,925 (Rodgers et al.) discloses a method and apparatus for processing an event occurrence within a multithreaded processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
March 28, 2007

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